| | Subclass | SSUE CLASSIFICATION | |
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| | Class | SSUE CLÆ | * |

PATENT NUMBER

U.S. UTILITY Patent Application

| O.I.P.E. | PATENT DATE |
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APPLICATION NO. CONT/PRIOR CLASS SUBCLASS ART UNIT EXAMINER BK 09/853999 716 2825 Rochit Rajsuman

Method of evaluating core based system-on-a-chip (SoC) and structure of SoC incorporating same

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| | ISSUING CLASSIFICATION | | | | | | | | | | | |
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| TERMINAL | DRAWINGS | | | CLAIMS ALLOWED | |
|---------------------------------------------------------------------------------------------------|-----------------------------------------------|-----------------------------------------|---------------------|---------------------------------------|------------------------------|
| ☐ DISCLAIMER | Sheets Drwg. | Figs. Drwg. | Print Fig. | Total Claims | Print Claim for O.G. |
| The term of this patent | | <u></u> | <u> </u> | NOTICE OF ALL | OWANCE MAILED |
| subsequent to (date) has been disclaimed. | (Assistant Examiner) | | (Date) | | |
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| not extend beyond the expiration date of U.S Patent, No. | | | | ISSI | JE FEE |
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| this patent have been disclaimed. | (Legal Instrume | ints Examiner) | (Date) | | |
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